WHAT IS CLAIMED IS:

1. A sub-assembly comprising a semiconductor chip and a chip carrier, said carrier comprising a) a core containing a voltage/ground plane, a first top signal plane forming the top of the core above the voltage/ground plane, the planes separated from one another by a layer of dielectric material; b) a second top signal plane above the first signal plane and separated from the first layer by a layer of dielectric material, and c) a conductive layer spaced from the second signal plane by a layer of dielectric material, the conductive layer forming the top surface of the carrier and being electrically coupled to the semiconductor chip positioned above the chip carrier, to deliver signals to and from the chip through the conductive layer to the top surface of the second signal plane; said chip having a planar surface, the edges of which create a footprint image on the carrier, the signals from the chip entering the carrier within the area of the footprint image, circuit lines on a surface of the second signal plane routing a first set of signals to a location outside the area of the footprint image and routing a second set of signals closer to an edge of the footprint area; the circuit lines coupled to microvias extending through the second signal plane down to the first signal plane, at least some of the second set of circuit lines being rerouted on the first signal plane to a location outside of the footprint area or to a location within the footprint area closer to an edge of the footprint area, the core having a plurality of conductive vias through which all of the signals are adapted to be transmitted between the chip and a printed wiring board.

2. The sub-assembly according to claim 1 wherein the core of the chip carrier further includes a first bottom signal plane below and separated from the at least one voltage/power plane by a layer of dielectric material, said carrier further including a second bottom signal plane beneath and separated from the first bottom signal plane by a layer of dielectric material, and a bottom conductive layer forming the bottom of the carrier adapted to be attached to a printed wiring board, and separated from the second bottom signal plane by a layer of dielectric material.

3. The sub-assembly according to claim 1 wherein the carrier is electrically coupled to the planar surface of the chip through a flip chip connector.

4. The sub-assembly according to claim 3 wherein the flip chip connector comprises a C4 connector.

5. The sub-assembly according to claim 1 wherein the carrier is adapted to be connected to the printed wiring board through a ball grid array.

6. The sub-assembly according to claim 2 wherein the dielectric layers separating the planes in the core are reinforced with glass fibers, and the dielectric layers separating the signal planes and conductive layers above and below the core are unreinforced.

7. The sub-assembly according to claim 1 wherein the second top signal plane has a top surface that contains a plurality of conductive pads, and the circuit lines on said signal plane are electrically coupled to the conductive pads by means of microvias passing through the pads down to the first signal plane.

8. The sub-assembly according to claim 1 wherein the circuit lines that are rerouted closer to an edge of the footprint area on the second signal plane and on the first signal plane are moved a distance of between about 200 microns and about 400 microns closer to the edge of the footprint area.

9. A method for increasing the number of signals passing between a semiconductor chip and a printed wiring board through a chip carrier, wherein the chip has a generally planar shape that creates an imaginary footprint area on a planar top surface of a carrier on which the chip is mounted and through which the signals pass between the chip and the chip carrier, wherein the chip carrier includes a core having at least one voltage/ground plane, a first signal plane spaced above and electrically isolated from the voltage/ground plane by a layer of a dielectric material, the carrier further including a second signal plane separated from the first signal plane and electrically isolated there from by a dielectric layer, and a top conductive layer electrically connected to the chip and separated from the second signal plane by a dielectric layer,

the method comprising the step of routing a first set of signals on the second signal plane to a location outside of the footprint area of the chip.

10. The method according to claim 9 including the additional step of routing a second set of signals on the second signal plane from within the footprint area to a location closer to an edge of the footprint area.

11. The method according to claim 10 further including the step of passing the second set of signals that have been routed closer to the edge of the footprint area on the second signal plane through microvias in the second signal plane to a surface of the first signal plane, and rerouting at least some of the second set of the circuit lines on the first signal plane to a location outside of an edge of the footprint area.

12. The method according to claim 11 comprising rerouting at least some other of the second set of circuit lines on the first signal plane closer to an edge of the footprint area.

13. The method according to claim 12 further including the step of routing additional signals to a location on the first signal plane outside of the chip footprint area.

14. The method according to claim 13 including passing all of the routed and rerouted signals through the carrier core to the printed wiring board.

15. The method according to claim 14 wherein the signals are routed and rerouted on the first and the second signal planes along conductive transmission lines on a surface of said planes.

16. The method according to claim 9 further including the step of routing at least some of the signals in the top conductive layer to a location outside of the footprint area or closer to an edge of the footprint area, and thereafter coupling these signals through microvias to the second signal plane.

17. The method according to claim 10 wherein the circuit lines on the surface of the first signal plane and on the second signal plane that are moved closer to an edge of the footprint area are moved a distance of between about 200 and about 400 microns.

18. An electronic package comprising:

a) a semiconductor chip having a given planar surface containing a plurality of solder members through which signals are passed;

b) a printed wiring board;

c) a substrate carrier having

1) at least one power plane,

2) at least a first top signal plane between the at least one power plane and the chip, and at least one bottom signal plane between the power plane and the printed wiring board,

3) a conductive plane between the first top signal plane and the semiconductor chip, said conductive plane in contact with the plurality of solder members on the planar surface of the chip,

4) circuit lines passing along and through the top signal plane for transmitting signals between the chip and the printed wiring board,

wherein the planar surface of the chip forms an imaginary footprint area on the substrate carrier, with edges defining the planar shape of the chip, and at least some of the circuit lines are fanned out on the surface of said first top signal plane from the imaginary footprint area toward an edge of the footprint area before passing through the at least one power plane.

19. The electronic package according to claim 18 wherein the substrate carrier includes a second top signal plane between the first top plane and the conductive plane, separated from both planes by a layer of dielectric material, wherein circuit lines are fanned out on the second top signal plane, some of them extending outside of the footprint area, and the fanned out circuit lines are then passed through the second top signal plane to the first top signal plane wherein any fanned out circuit lines that are within the footprint area are further fanned out on the first top signal plane whereby at least some of them extend outside of the footprint area, and all of the fanned out circuit lines are passed through the at least one power plane to the printed wiring board.

20. The electronic package according to claim 19 wherein additional circuit lines are fanned out on the first signal plane that are fanned out toward the edges of the footprint area on the second signal plane.

21. The electronic package according to claim 19 wherein the circuit lines are fanned out on the second signal plane a distance of at least between about 200 microns and about 400 microns toward the edges of the footprint area, and the circuit lines are fanned out on the first top signal plane a distance of between about 200 microns and about 400 microns toward the edges of the footprint area.

22. The electronic package according to claim 18 wherein the substrate carrier includes a core, and the last least one power plane is embedded in the core.

23. The electronic package according to claim 22 wherein the first top signal plane forms the top of the core.

24. The electronic package according to claim 18 wherein the substrate is electrically joined to the chip through a flip chip connection.

25. The method of making an electronic package composed of a semiconductor chip, a printed wiring board, and a chip carrier, wherein the chip carrier is coupled to the printed wiring board to transmit signals between said chip and said board, said chip having a

planar surface facing the carrier through which the signals are transmitted, said planar surface defined by edges delimiting an imaginary chip footprint area on the carrier the method comprising the steps of

a) forming a carrier core, said core composed of at least one voltage/power plane between a first top signal plane comprising the top surface of the core and a first bottom signal plane comprising the bottom surface of the core, and a dielectric material electrically isolating each of the planes from one another;

b) forming electrically conducting vias vertically through the core joining circuit lines on the first top surface to circuit lines on the first bottom plane;

c) laminating a second top signal plane on top of the first signal layer separated there from by a layer of dielectric material, and laminating a second bottom signal plane to the bottom of the first bottom signal layer, separated therefrom by a dielectric layer;

d) routing a first set of circuit lines on the second top signal plane to a location outside of the footprint area on the carrier, and routing a second set of circuit lines on the second top signal plane in closer proximity to the edges of the footprint area

e) forming microvias through the second top signal plane to the top of the vias in the core, and forming microvias extending from the bottom of the vias through the second bottom signal plane to the bottom conductive layer;

f) completing the assembly of the carrier by covering the second top signal plane with a layer of dielectric material, covering the second bottom signal plane with a layer of dielectric material, laminating the second top signal plane to a top conductive layer, and laminating the second bottom signal plane to a bottom conductive layer;

g) forming microvias from the top conductive layer down to the second top signal plane and forming microvias from the bottom conductive layer up to the second bottom signal plane;

g) electrically coupling the semiconductor chip to the top conductive surface of the carrier; and

h) electrically coupling the printed wiring board to the bottom conductive surface, whereby at least the first set of circuit lines that are routed on the top signal planes pass through the core outside of the footprint area, and at least some of the second set of circuit lines pass through the footprint in close proximity to the edges of the footprint area.

26. The method according to claim 25 including routing certain circuit lines on the top surface of the second top signal plane out of the footprint area and other circuit lines from within the footprint area to a location that is closer to the edges of the footprint area.

27. The method according to claim 25 including the additional step of routing circuit lines on the first signal plane away from the footprint area.

28. The method according to claim 25 wherein the chip carrier is electrically coupled to the chip through a flip-chip connection.

29. The method according to claim 25 wherein the carrier is electrically coupled to the printed wiring board through a ball grid array.

30. The method according to claim 25 wherein the circuit lines on the first top signal plane and the circuit lines on the second top signal plane that are routed closer to an edge of the footprint area are moved a distance on the respective surface of between about 200 microns and about 400 microns closer to the edges of the footprint area.